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| VLSI Design 6332 |
| Proposal |
| A Method to Implement Low Energy Read Operations, and Single Cycle Write After Read in Subthreshold SRAMs  by  The Sub-threshold Team  Author  Arijit Banerjee |

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| 11/8/2012 |

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Chapter 1

**Design Component, Research Component and Simulations for the Project**

Findings from the prior works:

In [1], from the Fig. 8 (a) of the [1] shows that the Monte Carlo (MC) data indicating “mean-3sigma” RSNM of ST is lying in between 50mV to 0mV and “mean – 3sigma” hold signal to noise margin (HSNM) lying nearby 100mV. On the other hand in Fig. 9 the “mean + 3sigma” Vmin looks like lying in between 350-400mV. Hence, from the process variation and robustness standpoint with 400mV of supply voltage the 3sigma worse case values indicate that there may be failures in the bitcell in below 350mV if fabricated.

In [2], from the Fig. 7 it can be seen that the 3sigma worst case Read and Hold SNM is not robust at all. With 300 mV supply the “mean – 3sigma” WSNM is around 100mV, and “mean + 3sigma” Hold SNM is about 85mV, and “mean – 3sigma” read SNM becomes negative.

In [5], the Fig. 6, 7, 8 and 9 shows RSNM distributions of the proposed bitcell versus standard 6T bitcell. It can be referred from the plots that at 400mV the worst case “mean – 3Sigma” RSNM is around 20mV, and due to this fact there can be read failures from the standpoint of process variation.

Our observation from studying the papers [1] to [6] is that below 400mV most of the published SRAM bitcells are having issues with robustness standpoint limited by the bitcells’ worse case RSNM, VDRV, RSNM, HSNM, VMIN perspective which may lead to failures if the supply voltage is lowered further in subthreshold domain. Hence, lowering dynamic energy consumption in SRAM by lowering supply voltage is been hindered by the poor robustness in below 400mV supply voltage in SRAM bitcells. Hence, we try to research other ways to mitigate energy consumption in sub-threshold SRAMs. The method mentioned in [3] as writeback is a common way to avoid the half select problem in subthreshold SRAMs.

The Proposal:

We propose a method to utilize the concept of writeback to implement low energy read operations. In our Method we implement 128bit intermediate latches in the global bitlines to latch all the 8 words (16 bits) in a single cycle write after read (writeback), and read operation, and if the user reads from the same row in two or more consecutive read operation, the Read Word Line (RWL) does not toggle and we just read from the intermediate latches. With this scheme we investigate the dynamic energy savings by not switching RWL and row decoders in the low energy read operations in which operating components of the memory are 16 bit output flip-flop, 128 to 16 bit bus interface logic, and input flip-flops only. We also investigate the effect of single cycle write after read over the half-select problem of SRAM bitcells in suthreshold supply voltages along with energy overhead or savings for this method. We plan to compare other methods for SRAM dynamic energy reduction with the proposed one in the next design review.

Motivation:

There was a version of sub-threshold data memory without column mux used in UVa Body Sensor Network (BSN) chip last year 2011. The memory had normal 128 bits of DIN and DOUTs directly providing to the user with operating voltage of 0.5 volt and frequency of 200 kHz. In the memory the writing operation was done in effective two cycles by write after read approach which is standard in sub-threshold memories to avoid the half select issue. Recently the BSN chip team has changed the BSN Instruction Set Architecture (ISA) along with the bus width of the main data and address bus to 16 bit each, and they demanded new features in the memory like somehow single cycle effectively writing, lowering the read dynamic power dissipation, and other features like including input and output flops, converting the existing 128bit bus to 16 bit bus interface to the SOC, and so on. In order to meet their requirements we added new circuits and modified the Data memory to meet the specification.

Design component, research component and simulations for the projects:

We tabulated the regular design components, research components and simulations to be done for the project as follows:



Chapter 2

**Proof of the Concept Simulation Figures and Corresponding Schematics**

For the proof of concept we provide the suggested pin description table, and timing diagrams, taken from “SRAM Specification Document November Test Chip 2012.doc” from BSN chip team followed by actual schematic and simulation figures, from the next page. Rest of this page is intentionally left blank for formatting. The pins correspond to the low Energy Read operations of the memory in the pin description table are BURSTENB and BURST\_RESET and the mode is called “BURST” in the SRAM Memory Specification Document.

**Pin Description Table for the DATA** **Memory:**

**** 

**Timing Diagrams for Read Operation:** The timing diagram provided represents two consecutive read operations and a write operation. Other internal signals like internal clock, internally latched DIN and ADR signal, and read word line (RWL) and write word line (WWL) are also specified for clarity.

CLK

ENABLEB

ADR

DOUT

DIN

READWB

Tacc

Tsu

Tsu

Tsu

Tsu

Th

Tcyc

Internal CLK

Internally Latched ADR

T\_Clk2ADR Internal

Internally Latched DIN

Internal RWL

RWL Pulse-width

Internal WWL

WWL Pulse-width

T\_Clk2DIN Internal

**Timing Diagrams for Write after Read Operation:** The timing diagram provided below represents two consecutive write after read operations and a read operation. Signals like internal clock, read word line (RWL) and write word line (WWL) are also specified. In the write after read operation the output bus retains the last state.

CLK

ENABLEB

ADR

DOUT

DIN

READWB

Tacc

Tsu

Tsu

Tsu

Tsu

Th

Th

Tcyc

Th

Last State

Internally Latched ADR

T\_Clk2ADR Internal

Internally Latched DIN

T\_Clk2DIN Internal

Internal RWL

Internal WWL

RWL Pulse-width

WWL Pulse-width

Internal CLK

**Internal Change of Waveforms for WR value change:**

CLK

Tcyc

WR

Tsu

Th

T\_Clk2WR Internal

Mode 00

Mode 01, 10, etc. > 00

READWB

Th

Tsu

RWL

WWL

RWL Pulse-width

WWL Pulse-width

Increased RWL Pulse-width

Decreased WWL Pulse-width

Internally Latched WR

Internal CLK

Annotated full schematic of 4KB subthreshold SRAM data memory:

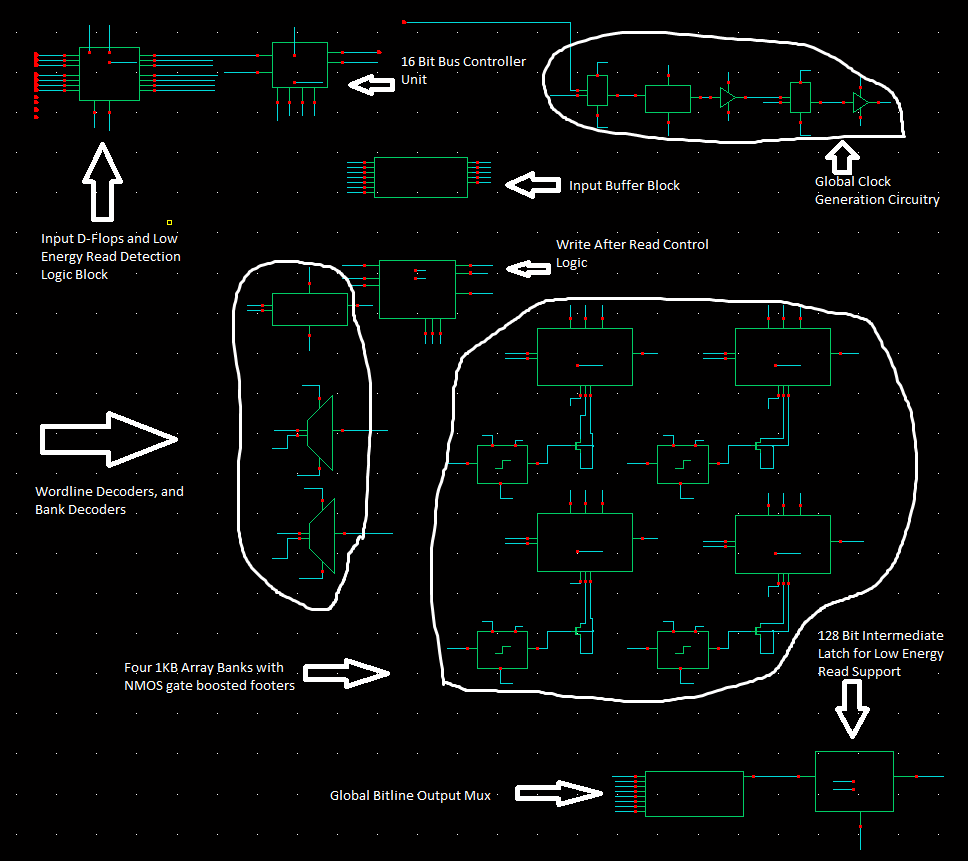


Fig. 1-a

Simulated and annotated waveform of the single cycle write after read, and normal read operations:

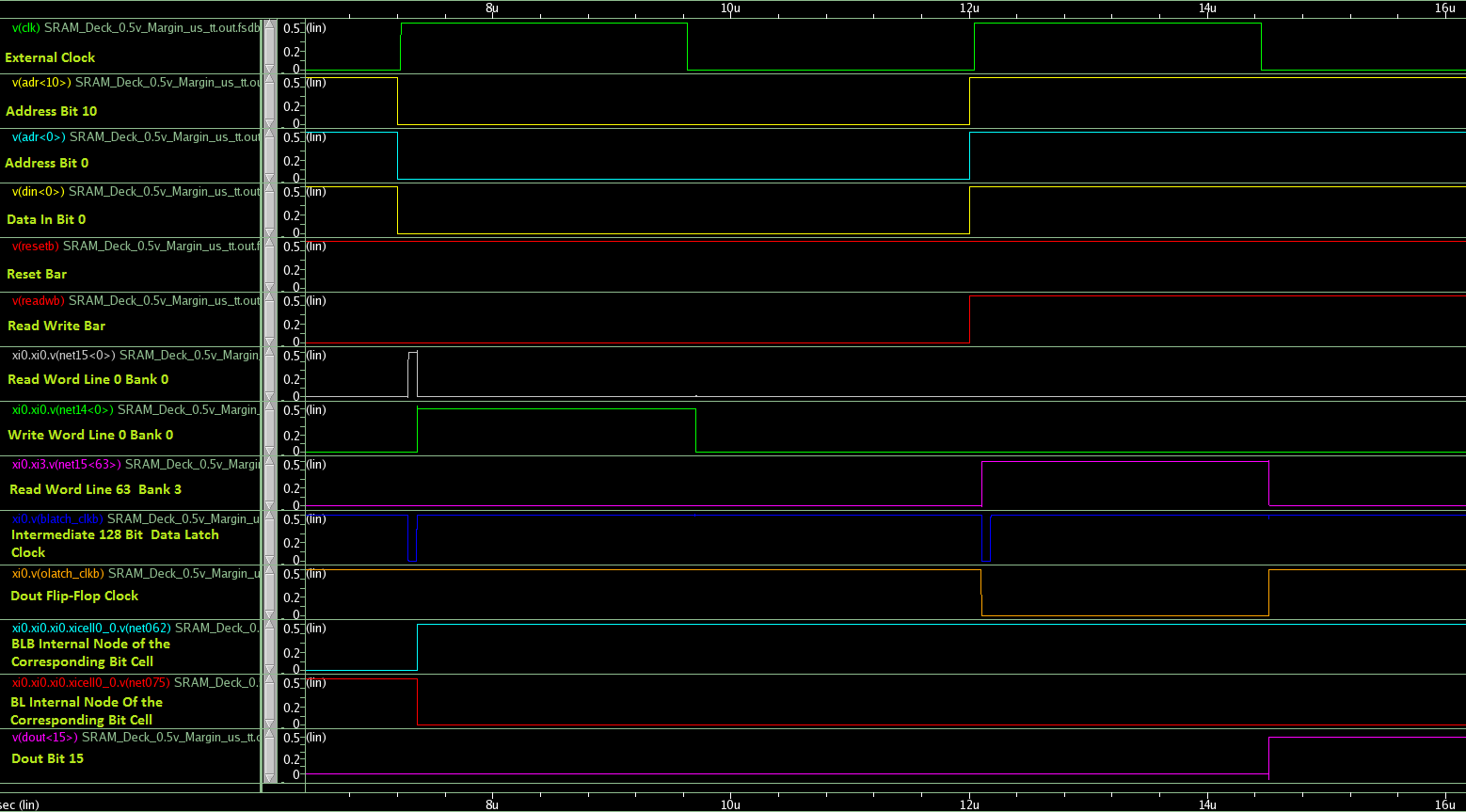


Fig. 1-b

Simulated and annotated waveform of the low energy read operations:

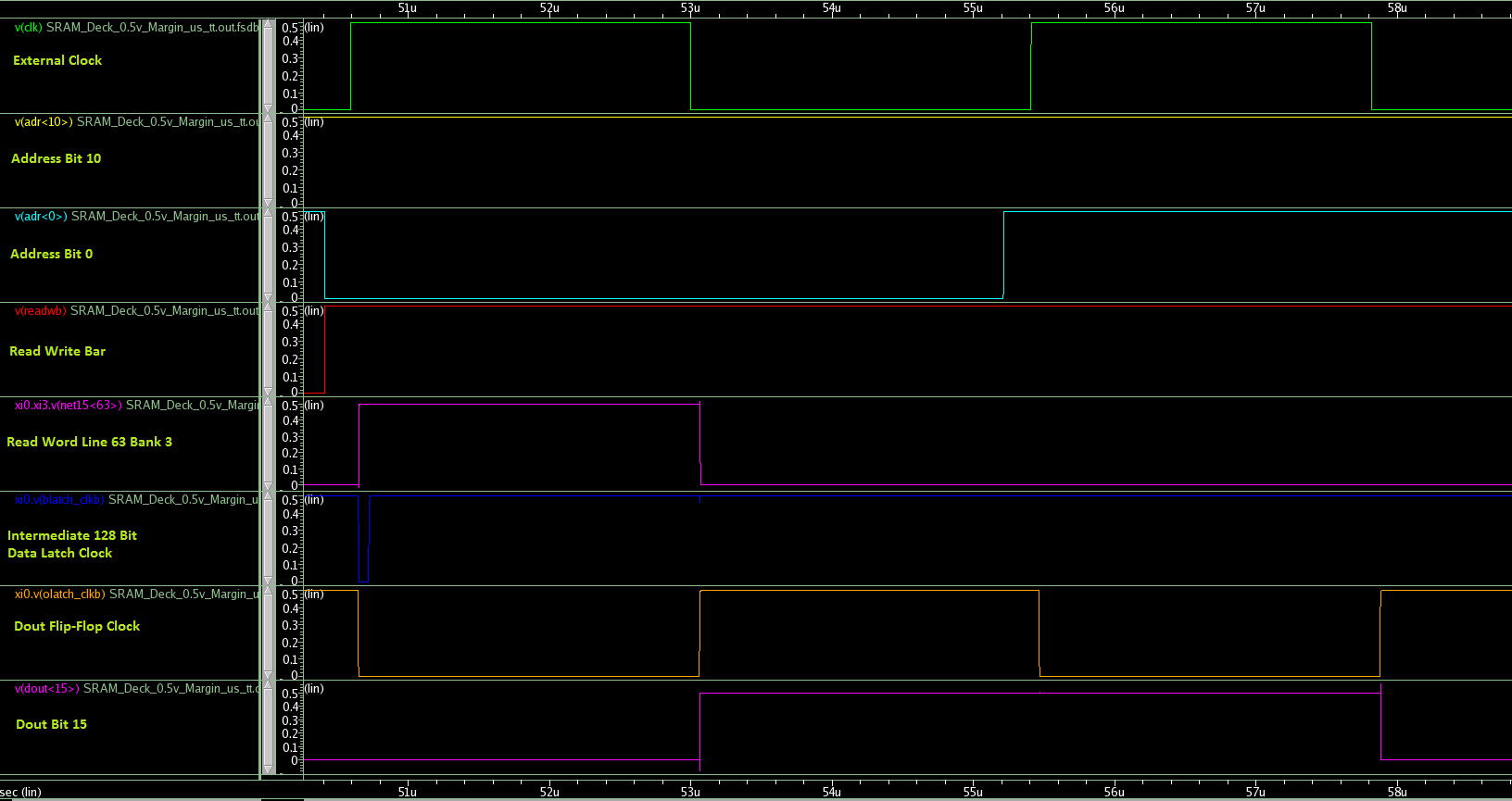


Fig. 1-c

Simulated and annotated waveform of the low energy read operations for energy measurement:

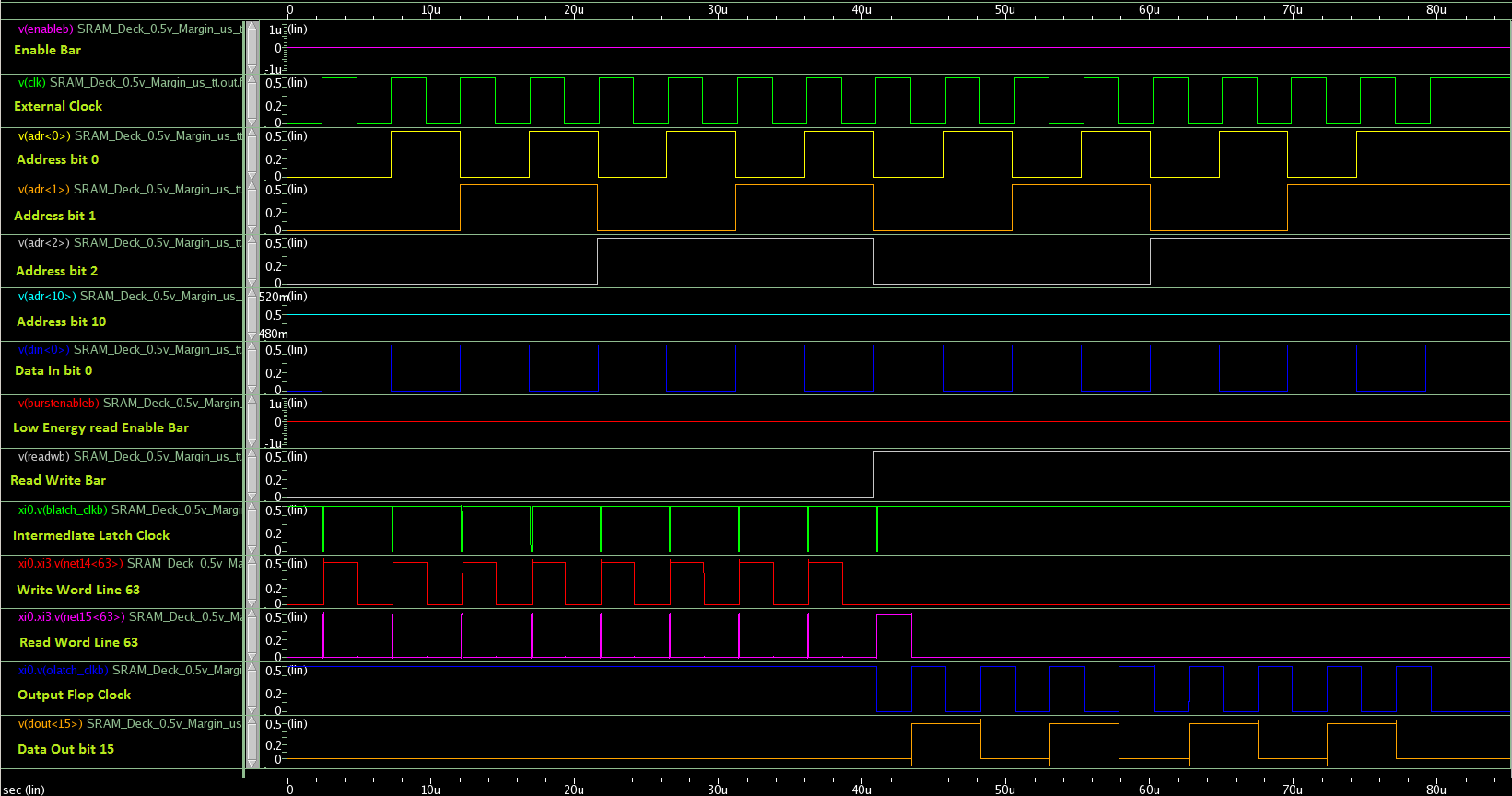


Fig. 1-d

Annotated schematic for low energy read operation support in 4KB subthreshold SRAM data memory :

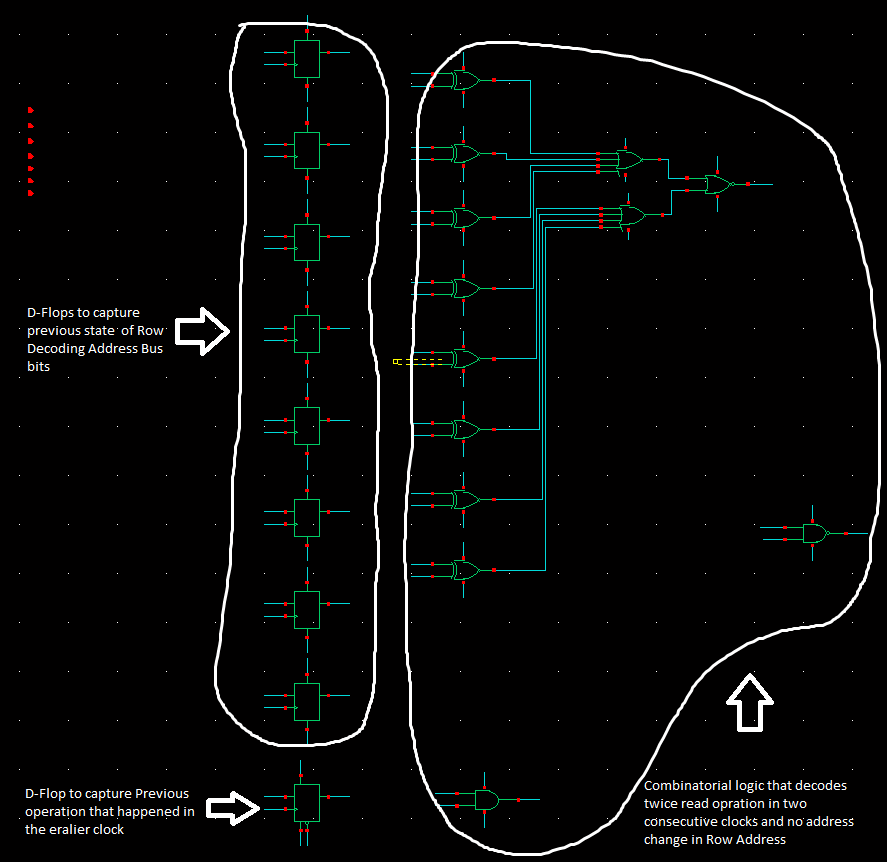


Fig. 2

Annotated schematic for single cycle write after read control logic, output-flop, and 128 bit intermediate latch clock generation logic in 4KB subthreshold SRAM data memory:

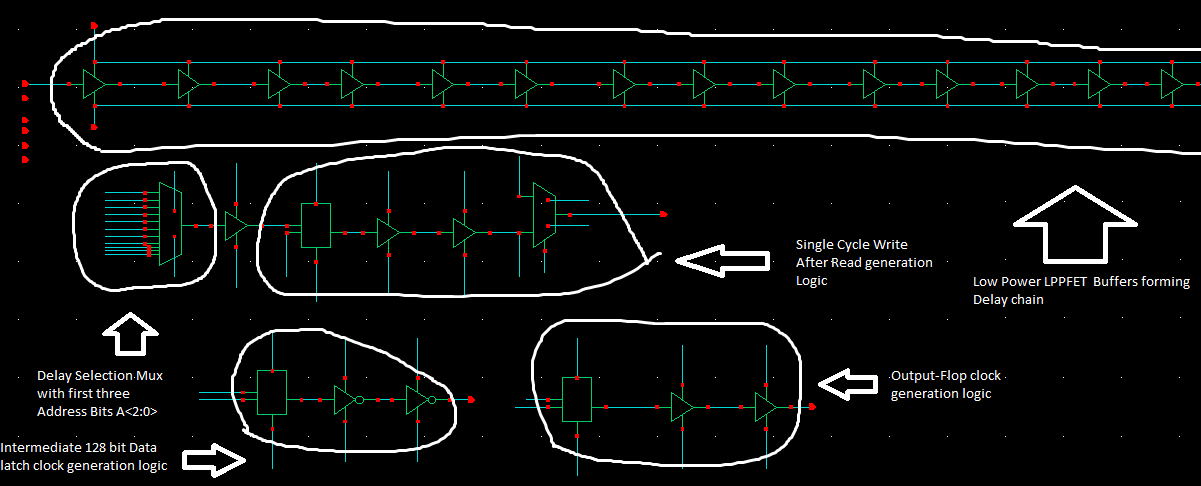


Fig. 3

16 bit bus controller and 128-to-16bit bus interface logic:

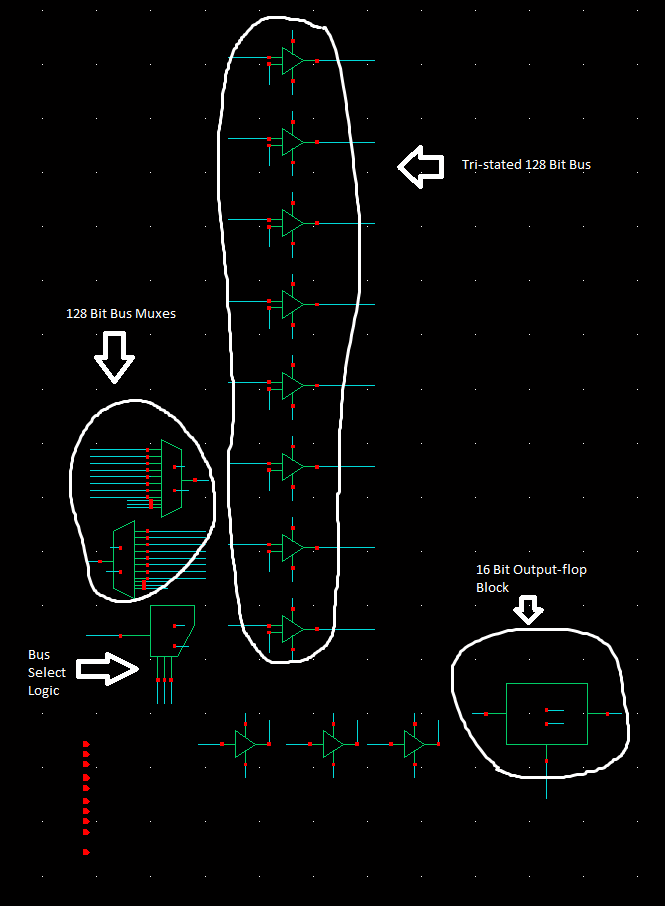


Fig. 4

Chapter 3

**Timeline for Project Completion and Intermediate Milestones**

Timeline and Milestone:

We already build these above sub-circuitry for low energy read operation support, single cycle write after read, 128 to 16 bit bus multiplexers, intermediate 128 bit latches and input and output flops. As this memory will always be operated at room temperature, we are simulating the same in 27C temperature only. We have simulated our sub-threshold memory in some PVTs including the PVT of TT\_0.5V\_27C corner and the functionality we are getting from simulation is what we intended. The supply voltage of 0.5V was chosen by the BSN chip group as the supply for the digital logic used is 0.5v. The memory is already been working with the supply voltage near by the “mean +3 sigma” DRV Vmin of the bitcell which is nearly 350mV. The timeline table provided for this project is as follows:

Timeline:



Chapter 4

**Results**

We simulated the low energy read operations preceded by the normal read operations and got the following table for energy savings in Joules. We used HSIM with highest SPICE accuracy.



For the robustness of the Write After Read operation, we tabulated the read word line and write word line pulse widths in valid Read and Write After Read operations for all WR<0:3> modes with TT and FF process corners, and marked failures in failed cases of functionality for internal SRAM margin issues as follows:



From the measurement we can see that in WR mode “000” the Memory functionality is “failed” in FF corner due to insufficient margin to generate read word line and write word line pulses correctly. Sill there are plenty of modes in those the SRAM operates successfully. Some of the simulation results are yet to be populated in SS, SF, and FS corners in those modes.

Chapter 5

**Remaining Task breakdown for group members**

Below is the Timeline-table including the name of the owner of each task: Here two tasks are performed solely by a BSN chip group member named Jim (James Boley) and another shared task, and he is not a member of the VLSI 6332 “Subthreshold Group.”



Chapter 6

**References**

[1] J. P. Kulkarni, K. Kim, and K. Roy, “A 160 mV Robust Schmitt Trigger Based Subthreshold SRAM,” *IEEE Journal of Solid-State Circuits*, vol. 42, no. 10, pp. 2303–2313, Oct. 2007.

[2] I. J. Chang, J.-J. Kim, S. P. Park, and K. Roy, “A 32 kb 10T Sub-Threshold SRAM Array With Bit-Interleaving and Differential Read Scheme in 90 nm CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 44, no. 2, pp. 650–658, Feb. 2009.

[3] T. H. Kim, J. Liu, J. Keane, and C. H. Kim, “A high-density subthreshold SRAM with data-independent bitline leakage and virtual ground replica scheme,” in *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*, 2007, pp. 330–606.

[4] B. H. Calhoun and A. Chandrakasan, “A 256kb sub-threshold SRAM in 65nm CMOS,” in *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*, 2006, pp. 2592–2601.

[5] G. K. Reddy, K. Jainwal, J. Singh, and S. P. Mohanty, “Process variation tolerant 9T SRAM bitcell design,” in *Quality Electronic Design (ISQED), 2012 13th International Symposium on*, 2012, pp. 493–497.

[6] Ali Valaee, Asim J. Al-Khalili, “SRAM Read-Assist Scheme for High Performance Low Power Applications” in *International SoC Design Conference (ISOCC), 2011,* pp. 179-182*.*